Bytesaver II

Instruction Manual

Five Dollars

CROMEMCO

BYTESAVER II

Instruction Manual

CROMEMCO, INC.
28Ø Bernardo Avenue
Mountain View, CA 94Ø4Ø

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Section 1

INTRODUCTION

This manual provides assembly instructions, operating instructions and theory of operation for the Cromemco BYTESAVER II memory board.

The BYTESAVER II is an S-100 bus compatible 8K-byte capacity 2708-type EPROM memory board and programmer. The BYTESAVER II features:

- Independent operation as an 8K-byte ROM memory board.
- Independent operation as a 2708 PROM programmer.
- BANK SELECT allowing memory expansion beyond 64K-bytes.
- Powerful DMA configuration options with DMA OVERRIDE.
- Fully buffered address lines.
- Digital count derived PROGRAM PULSES (no erratic one-shots).
- A memory protect switch for each ROM socket.
- All options switch selectable (no soldered jumper wires).

This manual consists of four basic sections: Operating Instructions, PROM Programming Instructions, Theory of

Operation and Assembly Instructions. If you purchased a BYTESAVER II kit, the Assembly Instructions provide step-by-step construction and initial test procedures. Section 2.1 of the Operating Instructions provides a BYTESAVER II operational overview for those who want to put the board quickly to use.

TECHNICAL SPECIFICATIONS

BYTESAVER II PROM CARD

MEMORY CAPACITY:	8K BYTES
MEMORY TYPE:	INTEL 2708 PROM OR EQUIVALENT
MEMORY ACCESS TIME:	450 NANOSECONDS
WAIT STATES @ 2 MHZ:	NONE REQUIRED
WAIT STATES @ 4 MHZ:	ONE PER MACHINE CYCLE
BUS COMPATIBILITY:	S-100
POWER REQUIREMENTS:	+8 VOLTS AT 0.8 AMPS (MAX.)
	+18 VOLTS AT 0.4 AMPS (MAX.)
	-18 VOLTS AT 0.2 AMPS (MAX.)
OPERATING ENVIRONMENT:	0-55 DEGREES CELSIUS

Section 2

OPERATING INSTRUCTIONS

Operating the BYTESAVER II board simply involves inserting from one to eight 27Ø8 PROM devices in sockets ROMØ - ROM7 (any sockets may be used or left unused), setting four switch groups to configure the board, plugging the board into a convenient S-1ØØ bus slot, then applying system power. To program a PROM, you will additionally need to run software described in Section 3, PROM PROGRAMMING INSTRUCTIONS.

2.1 SWITCH OPTIONS--AN OVERVIEW

The BYTESAVER II is configured by setting four switch groups located along the top edge of the board (see Figure 1). To provide an operational overview, and for later quick reference, the function of each switch is briefly explained in this section.

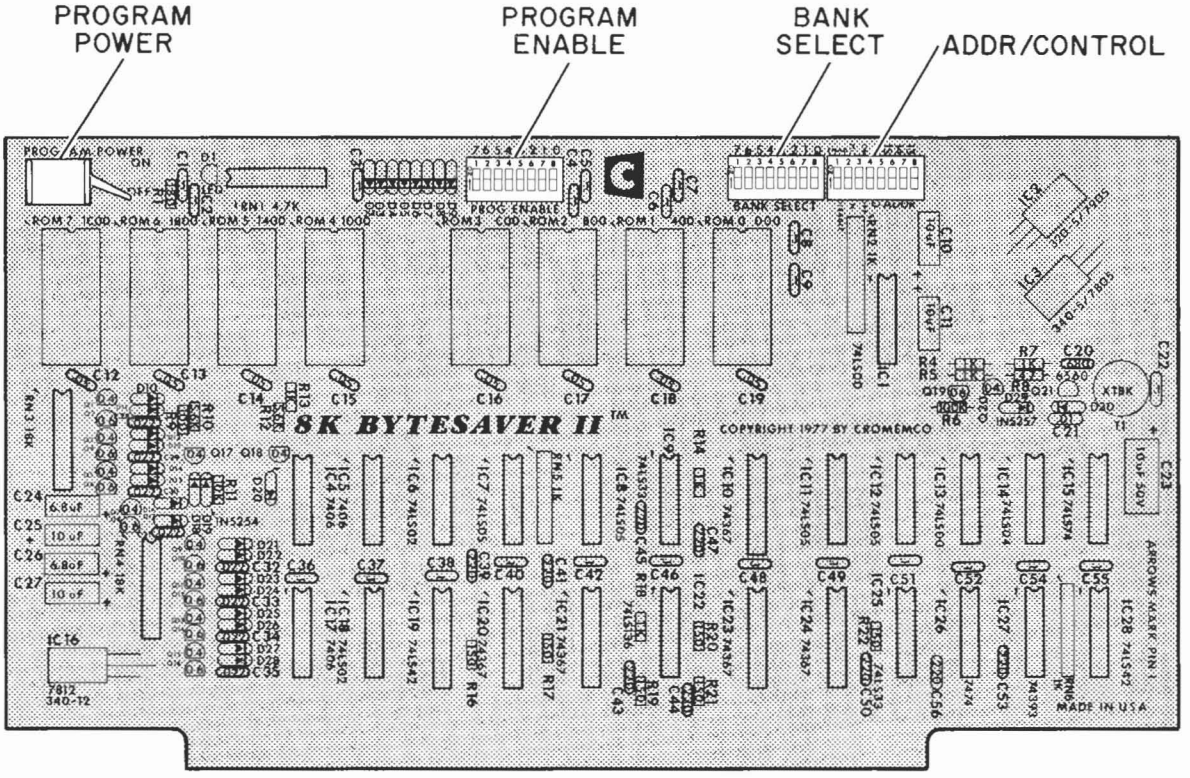


Figure 1: SWITCH LOCATIONS

- PROGRAM POWER TOGGLE SWITCH

The PROGRAM POWER switch turns the +33.5 volt dc to dc power supply ON and OFF. Position this switch ON before PROM programming; position it OFF when done to prevent inadvertent re-programming.

- PROGRAM ENABLE SWITCHES

The eight PROGRAM ENABLE switches individually enable and inhibit programming sockets ROMØ thru ROM7. An ON switch enables programming; an OFF switch inhibits programming. These switches may be alternately viewed as MEMORY PROTECT switches, preventing any memory write operations when in the OFF position.

To enable and disable socket programming, associate the board socket numbers (ROMØ - ROM7) with the numerals printed above the switch DIP (7 to the far left, Ø to the far right).

- BANK SELECT SWITCHES

The eight BANK SELECT switches map the BYTESAVER II into any combination of 64K-byte memory banks (bank Ø - bank 7). Setting a BANK SELECT switch ON logically places the board in the correspondingly numbered memory bank; an OFF switch logically removes the board from a bank. Again, associate the bank number with the numerals printed above the BANK SELECT switches, not the numerals on the DIP proper.

- ADDR/CONTROL SWITCHES

The ADDR/CONTROL switches control several different functions (see Figure 2).

The BANK ENABLE/DISABLE switch enables multiple 64K memory banks (bank Ø - bank 7) when ON, and disables multiple banks when OFF (normal direct 64K addressing).

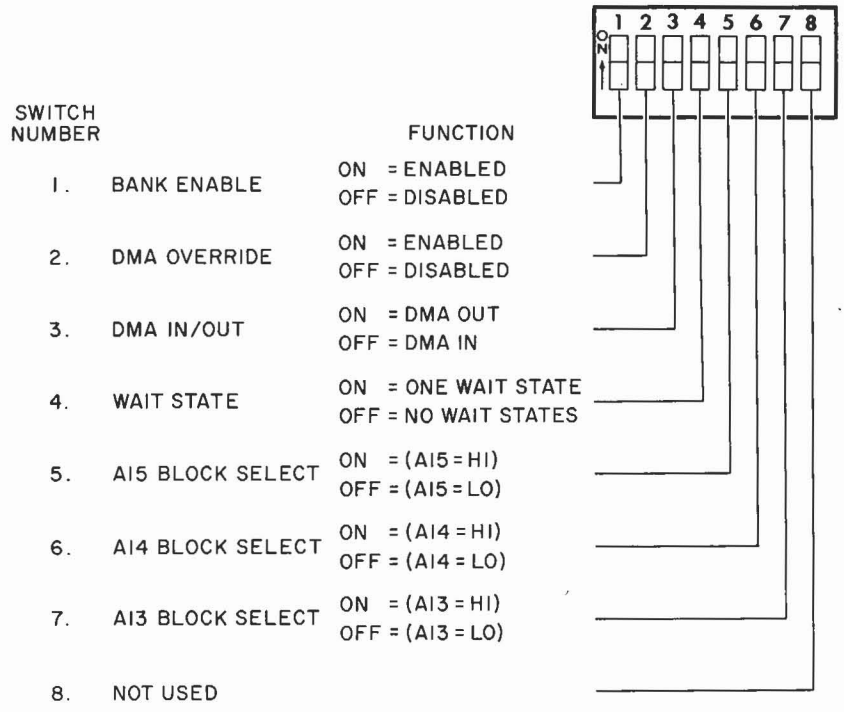


Figure 2: ADDR/CONTROL SWITCHES

The DMA ENABLE/DISABLE switch enables DMA OVERRIDE when ON and disables DMA OVERRIDE when OFF. For normal direct 64K DMA addressing, position the switch OFF. When performing DMA with memory banks enabled, turn the switch ON. The DMA IN/OUT switch is active only when DMA OVERRIDE is enabled. With DMA OVERRIDE enabled, the BYTESAVER II will respond directly to a DMA in the board's 16-bit address range by

board enabling if DMA is IN, and by board disabling if DMA is OUT, regardless of current active memory bank status at the time. This feature effectively permits the user to define one board out of several stacked in different memory banks as the DMA board (the one with DMA IN), and the boards in other memory banks as non-DMA boards (the ones with DMA OUT).

The WAIT STATE switch is used to match the CPU cycle time to the 27Ø8 PROM 45Øns (max) memory access time. Positioning the WAIT STATE switch ON introduces one wait state during each machine cycle; the OFF position introduces no wait states. When used in a Cromemco system with a ZPU running at 4 MHz, position the switch ON. The switch may be left OFF when operating at 2 MHz.

The three high order address select switches A13, A14 and A15 memory map the BYTESAVER II into one-of-eight 8K-byte memory "blocks". Setting all three switches OFF maps the BYTESAVER II into the lowest 8K-byte block of memory (ØØØØH - 1FFFH); setting all switches ON maps the board into the highest 8K-byte block (EØØØH - FFFFH).

EXAMPLE 1

Suppose you have a 4 MHz Cromemco system, and you want to memory map your BYTESAVER II into the highest 8K-byte memory block (E000H - FFFFH). As a standard practice, you decide to program 2708 PROMs in socket ROM7 only. Also assume there is no other memory overlapping the uppermost 8K of memory, so multiple memory banks are not required.

For memory read operation, the BYTESAVER II switch settings would then be as shown in Figure 3.

To program a 2708 PROM in socket ROM7, all switch settings remain the same except the PROGRAM POWER switch, which must be turned ON.

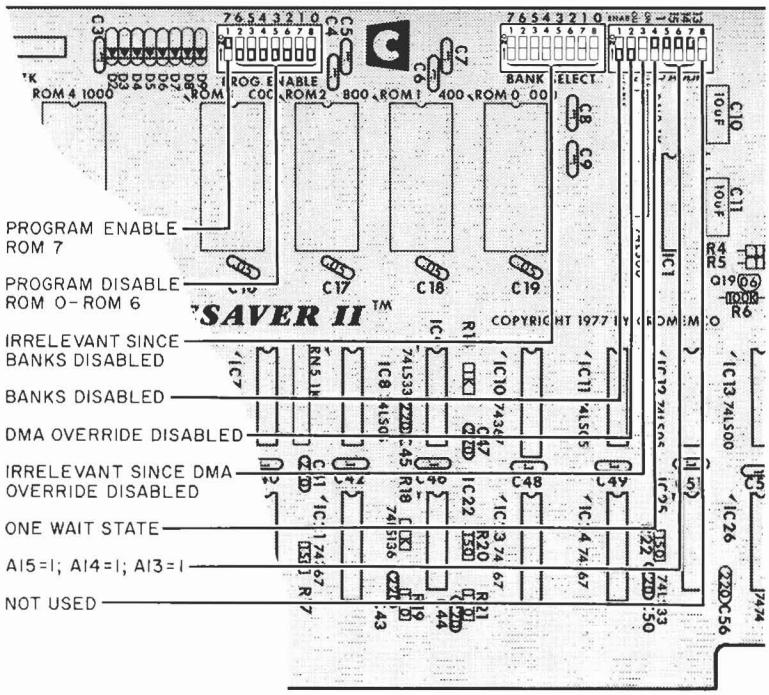


Figure 3: EXAMPLE 1 SWITCH SETTINGS

The following example illustrates all of the BYTESAVER II special features.

EXAMPLE 2

Suppose you set your Cromemco ZPU card for 2 MHz operation, and assign your BYTESAVER II to memory block 4 (8000H - 9FFFH). Again as a standard practice, you program 2708 PROMs in socket ROM7 only.

Also assume another Cromemco memory board with BANK SELECT exists for DMA transfers only in overlapping memory 8000H - BFFFH, bank 1 (a 16KZ RAM card, for example). You then decide to map the BYTESAVER II into memory bank 0 so that it will be enabled on a system RESET or a Power-ON Clear (see Section 2.5 for details).

The correct BYTESAVER II switch settings for this configuration are then shown in Figure 4.

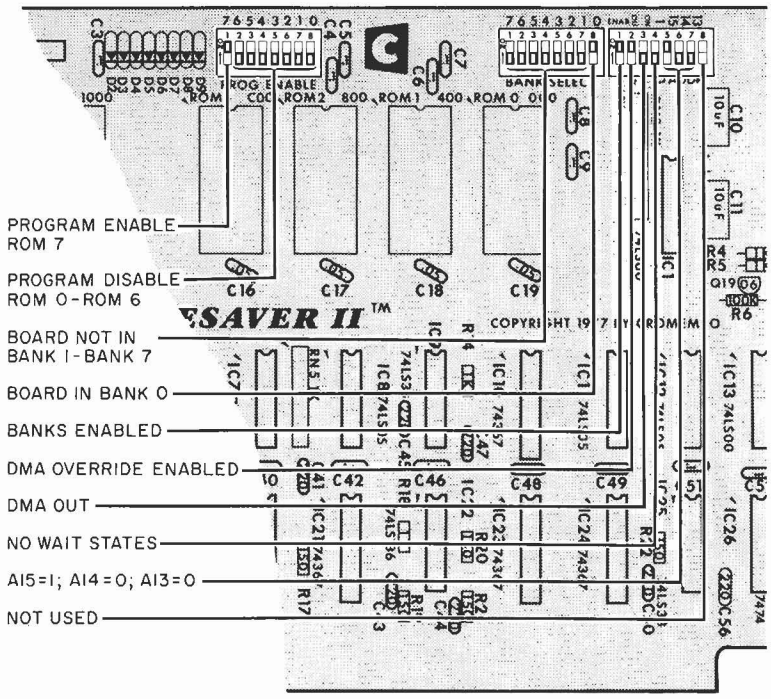


Figure 4: EXAMPLE 2 SWITCH SETTINGS

The sections which immediately follow discuss all of the

BYTESAVER II special features and operational modes touched upon in this section in greater detail.

2.2 ADDRESSING THE BYTESAVER II

Addressing a byte on the BYTESAVER II involves four levels of selection: choosing a memory bank, a memory board, an IC chip, and finally choosing the byte-on-chip.

Memory banks are addressed by the CPU outputting a control word to an integral OUTPUT PORT 40H contained on each BYTESAVER II board. Board, chip and byte-on-chip are all decoded from the sixteen bit address sent out by the CPU on the S-100 bus.

Since the board capacity is 8K bytes, board select is generated by the high order address lines A13, A14 and A15. There are eight ROM sockets, so the next three high order address lines A10, A11 and A12 are used to hardware generate chip enable (selecting ROM0 - ROM7), and the remaining ten address lines A0 - A9 are used to address one-of-1024 bytes on a 2708 PROM (see Figure 5).

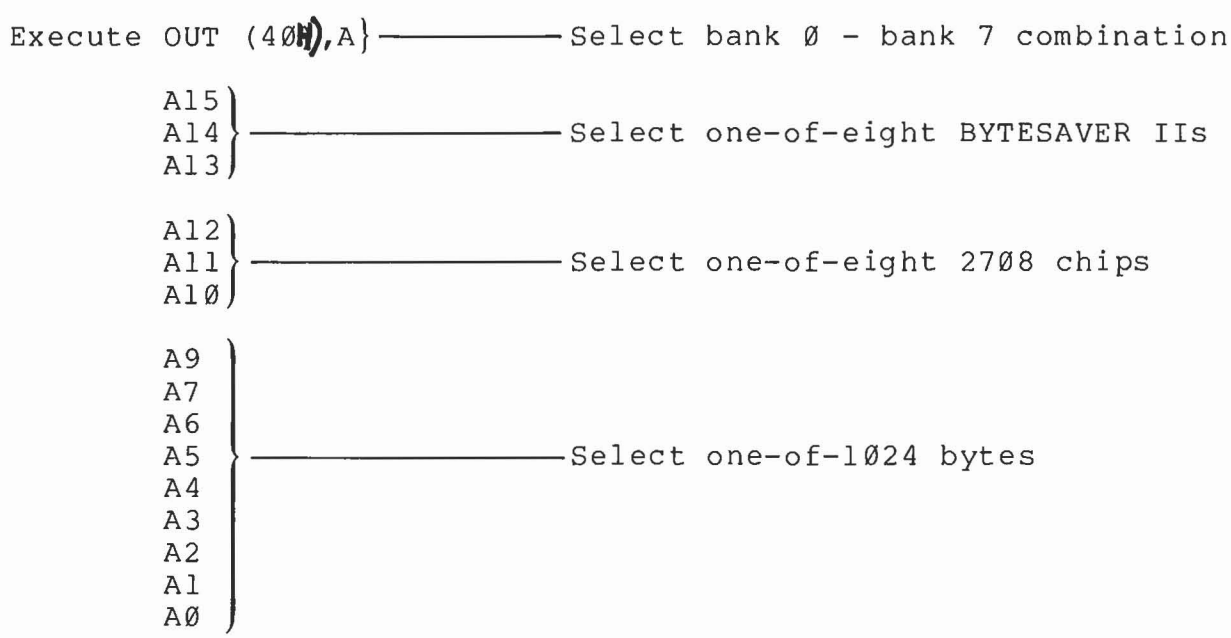


Figure 5: BYTESAVER II ADDRESSING

2.3 BOARD SELECT/CHIP SELECT

The three high order S-1ØØ bus address lines are hardware compared to switches A13, A14 and A15 in the ADDR/CONTROL switch group. Any switch ON corresponds to a selected logic 1 on its corresponding address line; any switch OFF selects a logic Ø on its corresponding address line. The eight switch setting combinations and their corresponding BYTESAVER II memory block assignments are tabulated below.

Table 1

SWITCH			BYTESAVER II MEMORY ASSIGNMENT	
A15	A14	A13		
OFF	OFF	OFF	0000 - 1FFF	;BLOCK 0
OFF	OFF	ON	2000 - 3FFF	;BLOCK 1
OFF	ON	OFF	4000 - 5FFF	;BLOCK 2
OFF	ON	ON	6000 - 7FFF	;BLOCK 3
ON	OFF	OFF	8000 - 9FFF	;BLOCK 4
ON	OFF	ON	A000 - BFFF	;BLOCK 5
ON	ON	OFF	C000 - DFFF	;BLOCK 6
ON	ON	ON	E000 - FFFF	;BLOCK 7

Each ROM socket ROM0 - ROM7 spans a 1K-byte swath of memory. Address lines A10 - A12 feed a one-of-eight decoder (IC19 in the BYTESAVER II Schematic) to generate select signals for each ROM socket. The entire 64K address space may then be spanned by eight BYTESAVER II boards. Figure 6 illustrates such an arrangement along with the address range spanned by each ROM socket.

EXAMPLE 3

Suppose you programmed four 2708 PROMs with Cromemco's Z-80 MONITOR and 3K Control BASIC. The Z-80 MONITOR spans addresses E000H - E3FFH, and Control BASIC spans E400H - EFFFH. To load these programs, you would then place the four programmed PROMs in sockets ROM0, ROM1, ROM2 and ROM3 on a BYTESAVER II assigned to E000H - FFFFH with A13=1, A14=1 and A15=1.

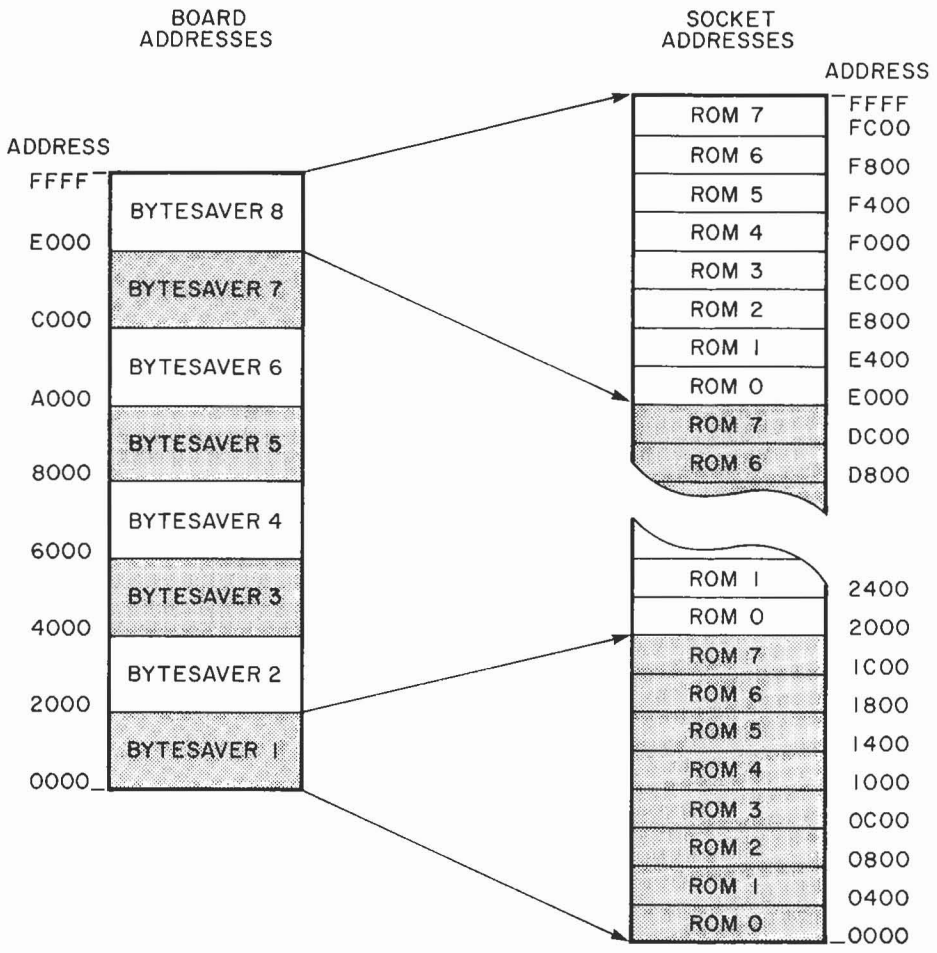


Figure 6: EIGHT BYTESAVER IIS SPANNING THE 64K ADDRESS SPACE

Carefully note that another memory module may <u>not</u> be mapped into the "hole" created by an empty BYTESAVER II ROM socket. The BYTESAVER II reads an empty ROM socket as memory data ØFFH, and actively drives the S-1ØØ DI bus lines DIØ - DI7 at logic 1 levels thereby creating a DI bus conflict when competing with another memory module.

2.4 MEMORY BANKS

BANK SELECT is an optional board feature which effectively allows memory expansion beyond the CPU's 64K direct addressing range. This feature may be completely disabled by switch selecting BANK DISABLE in the ADDR/CONTROL switch group. When this is done, the eight BANK SELECT switch settings become irrelevant. In this mode the BYTESAVER II exists only in the assigned 8K-byte memory block of the CPU's 64k direct addressing range for memory read, PROM programming and DMA operations.

To enable memory banks, switch select BANK ENABLE in the ADDR/CONTROL switch group. When this is done, the BYTESAVER II is logically placed in one or more 64K-byte memory banks with the eight BANK SELECT switches, and bank addressing is software controlled by executing the OUT (40H),A (or equivalent) Z-80 instruction.

Memory may be stacked up to eight banks deep (see Figure 7). Positioning one or more BANK SELECT switches ON places a BYTESAVER II in each corresponding memory bank. On the other hand, positioning all switches OFF completely removes the board from the memory map (except possibly for DMA transfers--see Section 2.6).

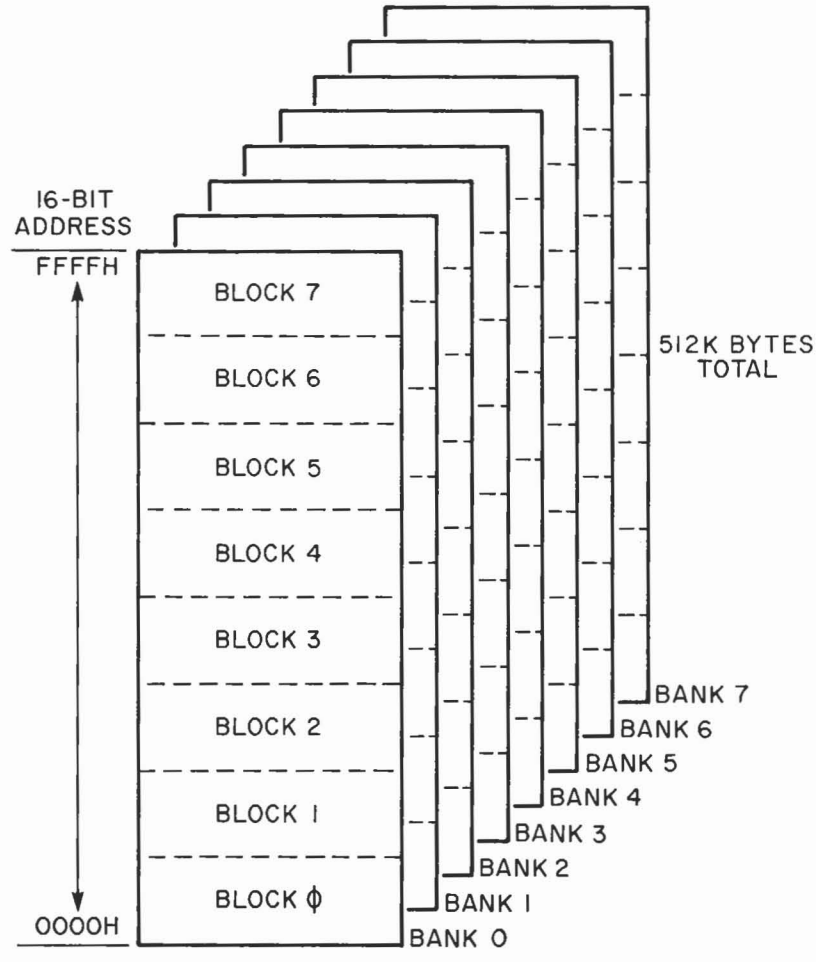


Figure 7: THE MEMORY MAP WITH MULTIPLE MEMORY BANKS

As stated above, memory banks are activated and deactivated under software control. Each BYTESAVER II contains an integral OUTPUT PORT 40H which latches the bits of the control byte output to it by the CPU. Each set bit (logic 1) enables its corresponding memory bank, and each reset bit (logic 0) disables its bank. Control byte bit 7 (MSB) controls memory bank 7, bit 6 controls memory bank 6, etc.

If the BYTESAVER II is switch mapped into any of the banks activated by the control byte (logical OR), the board responds when addressed and thus is placed "in" the memory map. When this condition occurs, the green LED indicator lights. Conversely, if the BYTESAVER II is switch mapped into no bank activated by the output control byte, the board will not respond when addressed and thus is "out" of the memory map. When a control byte inactivates the board, the green LED indicator goes out, and more specifically, the board responds by tri-stating (floating) all of its output lines. This behavior allows two or more memory boards with BANK SELECT to occupy the same or overlapping 16-bit address space but in different memory banks, provided only one board is memory bank active at a time, and all other boards are inactive. Memory bank conflicts may result if:

a) Two or more address overlapping memory boards are switch assigned to the same memory bank, or

b) Two or more 16-bit address overlapping memory boards assigned to disjoint memory banks are simultaneously activated by the same control byte.

EXAMPLE 4

Suppose two BYTESAVER IIs are both mapped into the uppermost 8K of memory, and their memory bank switches are set as shown in Figure 8. The resulting memory map is then shown in Figure 9.

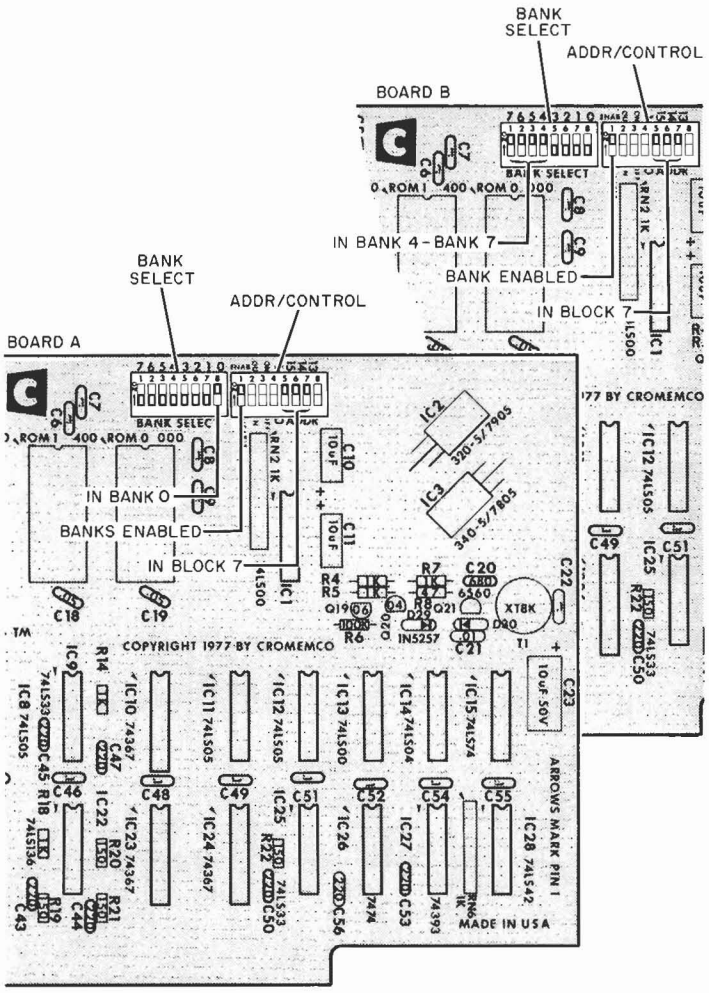


Figure 8: EXAMPLE 4 SWITCH SETTINGS

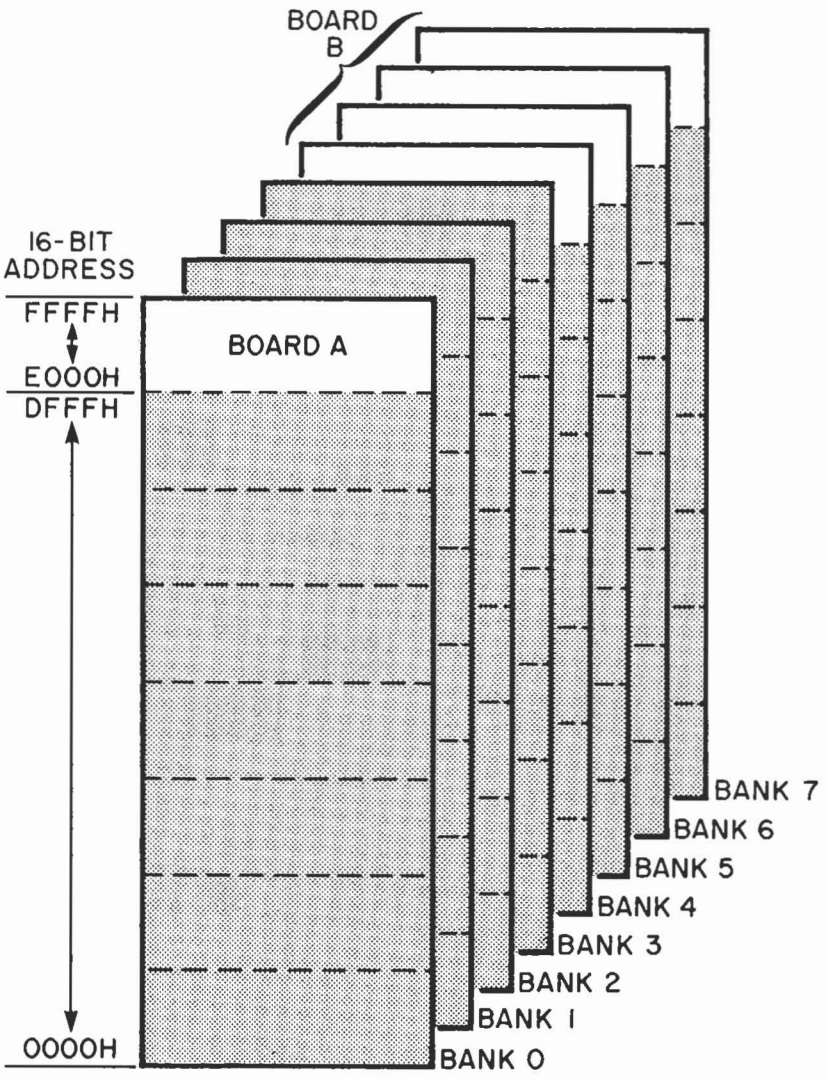


Figure 9: EXAMPLE 4 MEMORY MAP

To continue the same example, the sample programs below illustrate how to memory bank enable and disable the two boards.

• Executing the instructions below activates memory banks 2 and 3, and de-activates all other memory banks. The instructions then place both board A and board B in inactive memory banks (both boards inaccesible).

```
ADDR    OBJECT    MNEMONIC              COMMENT

0000    3E0C      LD   A,00001100B  ;LOAD 0000 1100 INTO REG. A
0002    D340      OUT  (40H),A      ;OUTPUT CONTROL BYTE TO PORT 40H
0004     --       --                ;NEXT INSTRUCTION
```

• Executing the instructions below simultaneously activates both boards A and B, and thus is <u>illegal</u>.

```
ADDR    OBJECT  MNEMONIC              COMMENT

0000    3E81    LD   A,10000001B   ;LOAD 1000 0001 INTO REG. A
0002    D340    OUT  (40H),A       ;OUTPUT CONTROL BYTE TO PORT 40H
0004     --     --                 ;NEXT INSTRUCTION
```

• Executing the instructions below places board A in an active memory bank, and board B in an inactive memory bank (board A available for memory read, PROM programming and DMA transfers; board B inaccessible).

```
ADDR    OBJECT  MNEMONIC              COMMENT

0000    3E01    LD   A,00000001B   ;LOAD 0000 0001 INTO REG. A
0002    D340    OUT  (40H),A       ;OUTPUT CONTROL BYTE TO PORT 40H
0004     --     --                 ;NEXT INSTRUCTION
```

• Executing the instructions below places board A in an inactive memory bank and board B in an active memory bank (board A inaccessible; board B available for memory read, PROM programming and DMA transfers).

```
ADDR    OBJECT  MNEMONIC              COMMENT

0000    3E60    LD   A,01100000   ;LOAD 0110 0000 INTO REG. A
0002    D340    OUT  (40H),A       ;OUTPUT CONTROL BYTE TO PORT 40H
0004     --     --                 ;NEXT INSTRUCTION
```

2.5 SELECT BANK Ø ON RESET OR POWER-ON-CLEAR (POC)

When system power is first applied, or after a subsequent system RESET, the BYTESAVER II will respond in one of two different ways. If multiple memory banks are DISABLED, the board will remain "in" the memory map in the CPU's 64K-byte direct addressing range.

If multiple memory banks are ENABLED, memory bank Ø is automatically hardware activated by a system RESET or a POC, and bank 1 - bank 7 are de-activated. Thus, a RESET or a POC to the boards in Example 4 would activate board A, and de-activate board B.

2.6 DIRECT MEMORY ACCESS

A device may request direct memory access to the BYTESAVER II by asserting the S-1ØØ bus line $\overline{\text{pHOLD}}$ low. The CPU grants the request by driving line pHLDA (hold acknowledge) high. When control line pHLDA is high, the device then may directly drive the S-1ØØ bus address lines and control lines (which are tri-stated during DMA transfers when pHLDA is high), and use the data bus lines for reading or writing without CPU intervention. The device may then transfer data at a rate limited only by the memory access time.

The general features of a DMA transfer are then:

- Fast asynchronous read or write access to memory.
- The DMA device should not be responsible for many overhead tasks (such as memory bank switching) to keep the memory access as quick as possible.
- The access is direct--no CPU intervention to slow the transfer.
- The DMA device must be capable of controlling and driving the tri-stated address, data and control busses.

In line with this general philosophy, the BYTESAVER II's DMA response behavior is controlled by two switches in the ADDR/CONTROL switch group; DMA OVERRIDE and DMA IN/OUT. There are four possible switch setting combinations; each is tabulated and discussed below.

Table 2

DMA OVERRIDE SWITCH	DMA IN/OUT SWITCH	BYTESAVER II RESPONSE
DISABLED	IN or OUT	Board enables when correctly addressed for either DMA or non-DMA transfers.
ENABLED	OUT	Board enables when correctly addressed for non-DMA transfers (normal operation); board disables during any system DMA transfer.
ENABLED	IN	Board enables when correctly addressed for non-DMA transfers; board enables when the DMA device addresses the board's assigned 8K block of memory, regardless of which banks were active before the DMA request.

The first table entry indicates the board behavior with DMA OVERRIDE DISABLED (note that in this case the DMA IN/OUT

switch setting is irrelevant). Here, the key phrase is "correctly addressed"; the BYTESAVER II will respond for memory read, write (PROM programming) or DMA transfers only when it is in an active memory bank (if multiple memory banks are enabled), and the S-100 bus address falls within the board's assigned 8K block of memory. The board in effect does not differentiate between a DMA data transfer and a normal read/write cycle in any way.

The BYTESAVER II does differentiate between DMA and non-DMA transfers with DMA OVERRIDE ENABLED, as shown in the last two table entries. A typical application demonstrating how DMA OVERRIDE works is shown in Figure 10.

Here, two BYTESAVER IIs are assigned to the same 16-bit address space with switches A13, A14 and A15; board A is assigned to memory bank 0, and board B to memory bank 1 (any other Cromemco memory boards with BANK SELECT and DMA OVERRIDE could also be used in the example). For non-DMA transfers, both boards are available for read/write operations when correctly addressed (board A is in memory bank 0 at E000H - FFFFH and board B is in memory bank 1 at E000H - FFFFH).

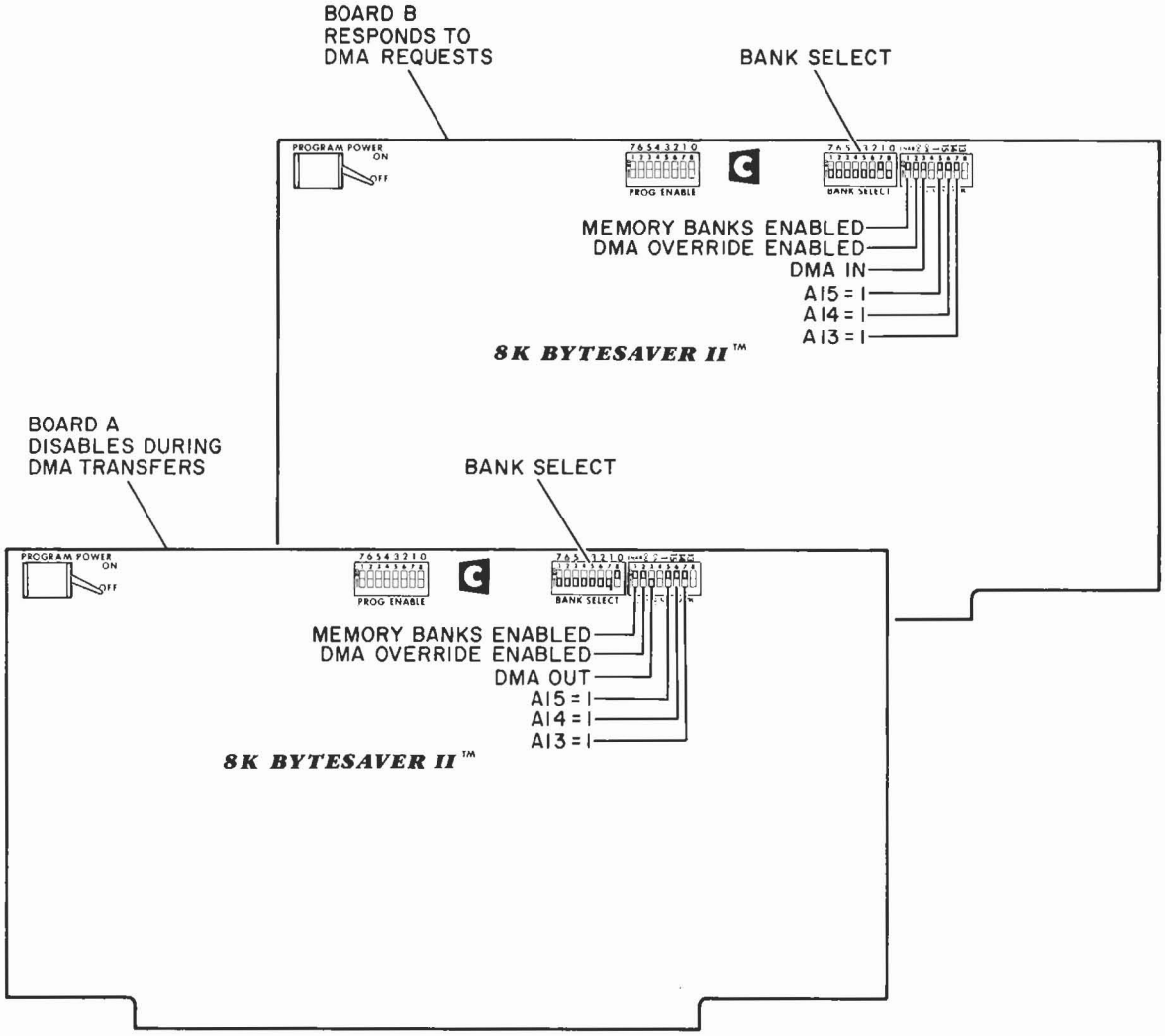


Figure 10: DMA OVERRIDE EXAMPLE CONFIGURATION

When the CPU grants an asynchronous DMA request by driving the pHLDA line high, board A automatically disables and board B enables when the S-100 bus address is in the range E000H - FFFFH, regardless of which board was in an active memory bank before the request.

Thus, the DMA OVERRIDE feature is seen as a means of overriding logical memory bank boundries during a DMA transfer. This provides a fast way of vectoring the DMA device to the DMA board (the one with DMA IN) and disabling all non-DMA boards (the ones with DMA OUT) without burdening the DMA device with any overhead memory bank switching responsibilities.

It should be noted that after the DMA transfer is completed, both BYTESAVER IIs revert back to the same memory bank status which existed before the DMA transfer.

Section 3

PROM PROGRAMMING INSTRUCTIONS

The 27Ø8 is an 8,192-bit ultraviolet light erasable and electrically programmable read-only memory chip. The 27Ø8 is erased, thereby forcing all bits to the logic 1 state, by exposing the chip's transparent quartz window to intense ultraviolet radiation. Consult the 27Ø8 manufacturer's literature for detailed erasure procedures.

To program a 27Ø8 PROM, insert an erased 27Ø8 into a PROGRAM ENABLED BYTESAVER II socket with the system power OFF, turn ON the system power, turn the PROGRAM POWER switch ON, then execute one of the Cromemco system programming commands described in the following sections. If the PROM is to remain in the same socket after programming, the socket should then be PROGRAM DISABLED. The PROGRAM POWER switch should be turned OFF after programming to prevent inadvertent re-programming of other PROMs on the board.

Each 27Ø8 byte is programmed by selectively changing logic 1 (erased) bits to the logic Ø state as required by the pattern being programmed. 27Ø8s may be re-programmed without intervening erasure provided no attempt is made to change logic Ø bits back to the logic 1 state--only complete EPROM erasure can force this transition.

The Cromemco PROM programming software described below writes a source code byte to each 2708 address in sequence. This process is then repeated until all 1,024 bytes of source code data have been written to the PROM 360 separate times. The BYTESAVER II responds to each memory write cycle by forcing the CPU into an idle state by asserting the CPU pRDY line low, driving the eight 2708 data output pins with the source code byte, and applying a digitally counted 192 usec PROGRAM PULSE (low for 16 usec, high for 176 usec) to the 2708 PROGRAM input pin while the $\overline{CS}$/WE line is held at +12 volts. Upon completion of the 192 usec interval, the pRDY line is again asserted high, and program execution resumes. Programming time for one 2708 is then approximately (192 usec/byte) x (1,024 bytes) x (360 programming passes) = 70 seconds.

Specific 2708 programming examples appear in the next three sections. Section 3.1 illustrates how to program 2708s using Cromemco's Z-80 MONITOR, DEBUG and ROS system commands, Section 3.2 discusses programming using 3K Control BASIC, and Section 3.3 illustrates how to program 2708s from Z-80 Assembly Language code.

3.1 PROGRAMMING FROM DEBUG, Z-8Ø MONITOR OR ROS

DEBUG (on disc package model FDA-S/L), Z-8Ø MONITOR (model number ZM-1Ø8) and ROS (model number ZA-8Ø8) all support a one line 27Ø8 programming command. The respective command formats are illustrated below:

```
-P EØØØ E3FF FCØØ<CR>              (DEBUG)
:P EØØØ E3FF FCØØ<CR>              (Z-8Ø MONITOR)
PROM,EØØØ,E3FF,FCØØ<CR>            (ROS)
```

where <CR> stands for pressing the RETURN key. Each command would result in programming a PROM located at FCØØH - FFFFH with source code located at EØØØH - E3FFH. Alternatively, these commands could have been entered as:

```
-P EØØØ SØØØ FCØØ<CR>              (DEBUG)
:P EØØØ SØØØ FCØØ<CR>              (Z-8Ø MONITOR)
PROM,EØØØ,SØØØ,FCØØ<CR>            (ROS)
```

using the swath operator.

The first two arguments in each command define the source code starting location and extent in memory. The source code location may be specified in terms of absolute addresses as in the first three examples, or in terms of a starting address and a swath width as in the last three. The third argument defines the 27Ø8 starting address on the

BYTESAVER II. The size of the source file (its swath width) and the 2708 starting address must be an exact multiple of 400H (the addresses must end in either 000H, 400H, 800H or C00H) or the command will be rejected and an error message issued.

After programming the 2708, the source code is compared to the PROM contents, and any discrepancies are printed out according to the format illustrated below:

```
E000 2C 2D FC00
E2BC 03 05 FEBC
E3FF C9 ED FFFF
```

This printout indicates the source code byte 2CH at E000H was incorrectly programmed into the 2708 as 2DH at address FC00H, etc. If there are discrepancies, often re-programming the 2708 with the same source code will change "stubborn" bits to their proper state. If there are no programming errors, the user is prompted for a new command.

EXAMPLE 5

Assume you have 2K-bytes of development software located at 1000H - 17FFH which you want to store in 2708 PROM. Two erased 2708s occupy sockets ROM6 and ROM7 on a BYTESAVER II assigned to memory area E000H - FFFFH.

To program the PROMs, you would then PROGRAM ENABLE sockets ROM6 and ROM7, turn the PROGRAM POWER switch ON, and issue one of the following commands, depending on which operating system is running:

```
-P 1000 17FF F800<CR>     or          (DEBUG)
-P 1000 S800 F800<CR>

:P 1000 17FF F800<CR>     or          (Z-80 MONITOR)
:P 1000 S800 F800<CR>

PROM,1000,17FF,F800<CR>   or          (ROS)
PROM,1000,S800,F800<CR>
```

After programming is complete, the PROGRAM POWER switch should be turned OFF.

Storing a disc file program in 2708 PROM is usually accomplished by reading the disc source file into RAM, then executing the DEBUG "P" (Program Proms) command to write the RAM data to PROM located elsewhere in memory. A potential problem exists when programming 2708s with a ".HEX" extension object file using this procedure.

Moving a source file from disc to RAM is accomplished using the "F" (specify file name) and the "R" (read disc file) DEBUG commands. These commands will attempt to load the .HEX file from the disc into RAM beginning at the address specified by the "ORG" statement contained in the source code. The address so defined may not be RAM at all, or the area specified may be inconvenient for other reasons. To circumvent this problem, the .HEX file should be read into a convenient RAM area by specifying an appropriate displacement as the argument of the DEBUG "R" command (see next example). For further details, refer to Cromemco's Macro Assembler Manual.

EXAMPLE 6

Suppose you have a program named SAMPLE which is "ORGed" at 9200H. You use Cromemco's ASMB program to create a .HEX object file on disc. You would like to read the .HEX file from the disc to RAM starting at 200H, and then to use this data to program a 2708 PROM residing at FC00H - FFFFH.

With DEBUG running, you would then type:

-FSAMPLE.HEX<CR>

This specifies the file name as "SAMPLE.HEX". Then type:

-R7000H **<CR>**

This reads the file from the disc with a displacement of 7000H. The displacement 7000H is added to the ORG operand 9200H to yield the loading point 9200H + 7000H = 10200H = 0200H when the carry is discarded. Then type:

-P 200 S400 FC00<CR>

This command programs the 2708 at FC00H with the source code located at 200H - 5FFH.

3.2 PROGRAMMING FROM 3K CONTROL BASIC

3K Control BASIC (model number CB-308) program text may be stored in 2708 PROM for subsequent loading and execution by issuing an "EPROM" direct command.

To SAVE a Control BASIC (CB) program in a 2708 PROM:

a) Determine the length of the CB program text using the CB SIZE function value.

b) PROGRAM ENABLE sockets containing erased 2708 PROMs.

c) Turn the PROGRAM POWER switch ON.

d) Issue an EPROM ppp command where "ppp" is the 2708 PROM starting "page" address.

e) After receiving a CB message indicating successful programming, turn the PROGRAM POWER switch OFF.

3K Control BASIC logically partitions memory into "pages", where 1 page = 256 bytes. Pages 0 and 1 (0000H - 01FFH) are not used by CB; pages 2 and 3 (0200H - 03FFH) are used for variables, the input buffer and the stack; pages 4 thru 31 (0400H - 1FFFH) are normally used for CB program text and arrays; and pages 32 on (2000H - end of user RAM) are normally used to save CB program files (see Figure 11).

The 'EPROM ppp' command is used to program 2708s with the CB text area for later execution, the 'LOAD ppp' command reads a file from memory back into the text area for editing, and the 'RUN ppp' command initiates execution of the program text located at page 'ppp'.

The page number arguments of the EPROM, RUN and LOAD commands are specified in decimal. For the EPROM command, the page argument is the starting address of erased 2708 PROM. This number must be a multiple of 4, and sufficient erased PROM should start at this address to contain all of the CB program text. If the CB text does not completely fill any 2708, the remainder of the PROM will be filled with data 00H, and thus the unused area is <u>not</u> available for other data or CB text.

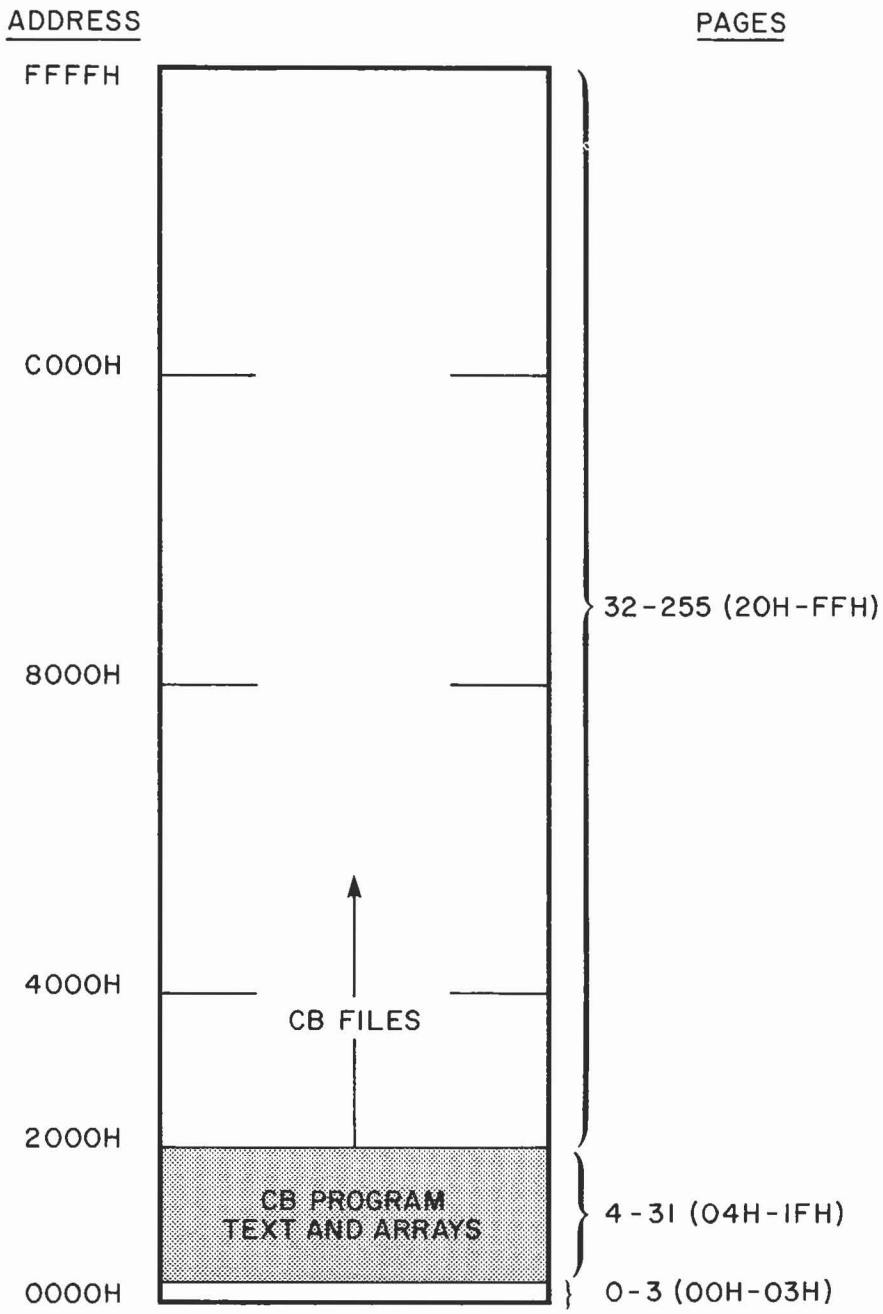


Figure 11: CONTROL BASIC MEMORY MAP

To determine the CB program text length, first clear the

text area with the NEW command, then execute the CB program shown below which evaluates and outputs the SIZE function value. The SIZE function evaluates to the number of bytes allocated to, but left unused by the CB program text.

```
>1 PRINT SIZE
>2 STOP
>RUN
 7142
```

The output (7,142 decimal in this example) gives the size of the unfilled CB text buffer. This number should be recorded for later reference. The size of the unfilled test buffer may be changed using the LOCK ppp command (see Cromemco's 3K Control BASIC Instruction Manual).

To determine the length of any CB program, load the same two statements at the beginning of your program (leave line numbers 1 and 2 free for this purpose), then RUN the combined program resulting in an output like that shown below:

```
>RUN
 5938
```

The program text length is the difference of these two numbers, or, 7142 - 5938 = 1204 bytes = 4.7 pages. A 4.7 page program would then require two 2708 PROMs (one would be completely filled with CB text; the other partially filled with CB text and the remainder filled with data 00H).

EXAMPLE 7

Suppose you wanted to store a 2,500 (decimal) byte CB program in 2708 PROM. Since 2,500 bytes = 9.8 pages, three 2708 PROMs are needed to store the text. Assume three erased PROMs occupy PROGRAM ENABLED sockets ROM5, ROM6 and ROM7 on a BYTESAVER II assigned to the uppermost 8K of memory . The PROMs then reside at F400H - FFFFH, or pages 244 - 255 decimal. You would then turn the PROGRAM POWER switch ON, and issue the command:

```
>EPROM 244
```

The programming time is approximately 70 seconds/PROM, so after about 140 seconds, you would see the message;

```
SAVED ON PAGE %F4 TO %FF

OK
>
```

if the programmed PROMs verified correctly, or;

```
SORRY

OK
>
```

if they did not. If the PROMs do not verify, you may try to re-program them with another EPROM 244 command without damage to the devices, or erase them and try again. Turn OFF the PROGRAM POWER switch after programming.

Assume now you move the three PROMs to sockets ROM0, ROM1 and ROM2 (E000H - EBFFH or pages 224 - 235) for running. Sockets ROM0, ROM1 and ROM2 should be PROGRAM DISABLED to prevent inadvertent re-programming. To run the program, issue the command:

```
>RUN 224
```

Or, to bring the program into the text area for editing, type:

```
>LOAD 224
```

3.3 PROGRAMMING FROM Z-80 ASSEMBLY CODE

Moving individual bytes or blocks of system memory to 2708 EPROM is most easily accomplished using DEBUG, Z-80 MONITOR or ROS system commands (see Section 3.1), but there may be instances where it is desirable to program 2708s during the execution of your own Z-80 assembly language program. This section discusses a relocatable Z-80 assembly language example program which may easily be modified to meet your specific requirements.

EXAMPLE 8

Assume you want to store source code data residing at 200H - 8FFH in 2708 PROM. This represents 1,792 bytes of data, so two 1,024-byte capacity 2708s are needed to store the data. In anticipation of later re-programming, the unused portion of the second device should be filled with data FFH. Thus, you fill source code area 900H - 9FFH with data FFH.

The example program assumes two erased 2708 PROMs occupy PROGRAM ENABLED sockets ROM6 and ROM7 on a BYTESAVER II assigned to the uppermost 8K of memory. Thus, the PROMs span memory addresses F800H - FFFFH. Before the program is run, the PROGRAM POWER switch should be turned ON.

```
;
;                2708 EPROM PROGRAMMER
;
;        THIS SAMPLE PROGRAM PROGRAMS TWO 2708 PROMS
;        IN SOCKETS ROM6 AND ROM7 ON A CROMEMCO
;        BYTESAVER II MEMORY BOARD.  THE SOURCE CODE
;        IN THIS EXAMPLE IS ASSUMED LOCATED AT 200H - 9FFH.
;
      (0200)  SOURCE:  EQU  200H          ;SOURCE CODE START ADDR
      (0800)  SWATH:   EQU  800H          ;SOURCE CODE LENGTH
      (FC00)  EPROM:   EQU  0FC00H        ;2708 PROM START ADDR
0000  210002  PGM2708: LD   HL,SOURCE     ;LOAD SOURCE ADDR,
0003  1100F8          LD   DE,EPROM       ;2708 START ADDR,
0006  010008          LD   BC,SWATH       ;AND SWATH FOR BLOCK XFER
0009  EDB0            LDIR                ;WRITE SOURCE TO 2708
000B  E5              PUSH HL             ;SAVE LAST SOURCE+1 ADDR
000C  2A2B00          LD   HL,(PASSES)    ;GET PROGRAMMING PASS#
000F  2B              DEC  HL             ;DECREMENT IT
```

```
0010 7C                 LD    A,H             ;TEST FOR PASS#=0000H
0011 B5                 OR    L               ;VALID ZERO FLAG
0012 222B00             LD    (PASSES),HL     ;RESTORE PASS#
0015 E1                 POP   HL              ;RESTORE LAST SOURCE+1
0016 20E8               JR    NZ,PGM2708      ;PASS# NOT 0000H--GO BACK
0018 010008             LD    BC,SWATH        ;DONE--READY TO VERIFY
001B 2B                 DEC   HL              ;POINT TO LAST SOURCE ADDR
001C 1B      VERIFY:    DEC   DE              ;POINT TO LAST 2708 ADDR
001D 1A                 LD    A,(DE)          ;GET 2708 BYTE AND
001E EDA9               CPD                   ;COMPARE TO SOURCE BYTE
0020 E22800             JP    PO,EXIT         ;DONE IF (BC)=0000H
0023 28F7               JR    Z,VERIFY        ;BYTES MATCH--NEXT BYTE
0025 3EFF    ERROR:     LD    A,0FFH          ;MISMATCH--LOAD REG. A
0027 76                 HALT                  ;WITH FFH AND HALT
0028 3E00    EXIT:      LD    A,00H           ;SUCCESS--LOAD REG. A
002A 76                 HALT                  ;WITH 00H AND HALT
002B 6801    PASSES:    DW    360             ;INITIAL PASS#=360
002D                    END   PGM2708
```

The sample program defines the source code starting address in register pair HL, the 2708 PROM starting address in register pair DE and the source code length (the byte count) in register pair BC. The program then block moves the source code to PROM 360 times by repeatedly executing the LDIR instruction. After the 2708 is programmed, the program then verifies the PROM contents against the source code. If they match, the program HALTs with 00H in Reg. A; if any byte does not match, the program HALTs with FFH in Reg. A. In actual use, the HALT instructions would be replaced by a branching instruction to the next code segment. The program may easily be placed elsewhere in memory provided the absolute jump instruction is re-assembled to point to the new EXIT point. It is the user's responsibility to test the contents of Reg. A for successful verification and take the appropriate action.

Section 4

THEORY OF OPERATION

This section gives a summary analysis of the BYTESAVER II at the component level. The user may find the section useful for troubleshooting the board, or just for gaining a fuller understanding of the board's features. The analysis is functionally divided into five categories: power supplies, addressing, memory read cycles, memory write cycles and DMA cycles. Refer to the BYTESAVER II Schematic for the following discussions.

4.1 POWER SUPPLIES

Unregulated +8 volt, +18 volt and -18 volt S-100 bus lines are voltage regulated to +5 volts, +12 volts and -12 volts by IC3, IC16 and IC2 respectively. The +5 volt line is also dc to dc converted to +33.5 volts by relaxation oscillator Q19, Q20, Q21, T1 and associated circuitry. The converter is turned ON and OFF by the PROGRAM POWER switch. The +33.5 volt line is Zener regulated to +27 volts by diode D19 which in turn provides the +26 volt (nominal) 2708 PROM programming voltage level.

If +33.5 volts is not present across C23 when the PROGRAM POWER switch is ON, check the collector of Q21 for a 0 volt/ 18 volt square wave running at between 150 and 250

KHz. If no switching voltage is present, check Q21 first. If Q21 is good, then check the other converter components Q19, Q20, D29 (a 1N5257, 33 volt Zener diode), D30 and T1 for opens and shorts.

4.2 ADDRESSING

High order address lines A13, A14 and A15 are compared to switches A13, A14 and A15 in the ADDR/CONTROL group by IC22. The comparison output [IC22 pin 3] is logically ANDed with S-100 bus signals and board signal [IC1 pin 3] to yield the important node signal BOARD ENABLE which logically equals the following Boolean expression:

BOARD ENABLE = (A13, A14, A15 MATCH) AND ($\overline{\text{sINTA}}$) AND ($\overline{\text{sOUT}}$) AND ($\overline{\text{sINP}}$) AND ($\overline{\text{MEMR DISABLE}}$) AND ($\overline{\text{IC1 PIN 3}}$) AND ($\overline{\text{sWO}}$ OR PROGRAM POWER)

The board will be enabled when the logic expression above is true, or evaluates to logic 1. The line [IC1 pin 3] will be low when the board is in an active memory bank, or has DMA IN during a DMA cycle.

Address lines A10, A11 and A12 feed one-of-eight decoder IC19 which generates chip select signals for each of the eight ROM sockets. Buffered address lines A0 - A9 parallel

feed all 2708s to finally select the byte-on-chip.

The board is mapped into an active or inactive memory bank by outputting a control word to output port 40H. Port address 40H is decoded from address lines A0 - A7 by the wire-ORed 7405's IC7 and IC8. These outputs are logically ANDed with control signals sOUT, pWR and switch BANK ENABLE to yield node signal BANK SELECT ENABLE = (sOUT) AND (pWR) AND (BANK ENABLE) AND (A0 - A7 = 40H). A high BANK SELECT ENABLE strobes a D-type flip flop at [IC26 pin 3] (it is also strobed on a Power-On Clear and a system RESET), and if the D-input at [IC26 pin 2] is low, the board is mapped into an active memory bank and the green LED indicator lights. If the D-input is high when strobed, the board is mapped into an inactive memory bank and the LED goes out.

The bits of the control byte output to port 40H are inverted by IC11 and IC12, and those bits selected with the BANK SELECT switches are logically ANDed to drive the D-input [IC26 pin 2]. Any logic 1 control bit output to port 40H which is switch connected to [IC12 pin 13] will then place the board in an active memory bank.

4.3 MEMORY READ CYCLES

The CPU begins a memory read cycle by placing the memory address on the S-100 address bus A0 - A15 and by asserting the sMEMR control line high. After sampling the pRDY line to ascertain whether the memory is ready to supply the data byte, the CPU strobes the data from the DATA IN bus DI0 - DI7 with a momentary high transition on the pDBIN line if memory is ready, or if memory is not ready, the CPU re-samples the pRDY line one clock cycle later.

If no wait states are selected with the WAIT switch in the ADDR/ CONTROL group, the pRDY line to the CPU stays high; if one wait state is selected with the switch, flip flop output [IC15 pin 8] goes low during pSYNC at the beginning of the read cycle (forcing pRDY = low), then goes high again one machine cycle later when pSYNC = low.

When the CPU asserts pDBIN high to strobe the read data from the DI bus, this signal is logically ANDed with BOARD ENABLE to yield signal $\overline{\text{DATA OUT ENABLE}} = \overline{(\text{pDBIN}) \text{ AND } (\text{BOARD ENABLE})}$. $\overline{\text{DATA OUT ENABLE}}$ in turn enables tri-state drivers IC24 which place the 2708 data byte onto the DI bus.

4.4 MEMORY WRITE CYCLES

The CPU begins a memory write cycle to the BYTESAVER II by placing the byte address on the S-1ØØ address bus AØ - A15 and asserting control signals sWO low and MEM WRITE high. The CPU then places the data byte on the data out bus DOØ - DO7, asserts the pWR line low and samples the pRDY line. If the pRDY line is low indicating memory has not latched the data byte, the CPU waits an integral number of clock cycles with stable address, data and control signals until the pRDY line again goes high. After the pRDY line is sampled high, program execution resumes.

The coincidence of MEM WRITE and BOARD ENABLE drives [IC13 pin 11] low, which releases the clear lines of counter IC27, gates the data byte to the 27Ø8 data output pins DØ - D7 thru drivers IC1Ø and IC23, and applies +12 volts to the appropriate PROGRAM ENABLED ROM socket CS/WE line by turning ON transistor Q18.

The dual 4-bit counter IC27 is driven by a 1 MHz clock which is derived from the 2 MHz $\overline{\text{CLOCK}}$ line from divide-by-2 flip flop IC26. The counter outputs are conditioned by one-of-ten decoder IC28 and flip flop IC15 to generate a PROGRAM PULSE waveform which is low for 16 usec and high for 176 usec at [IC4 pin 8]. This waveform turns transistor Q17 ON and OFF, which, in conjuction with Zener diode D19 (a 27 volt 3%

1N5254), supplies a 26 volt pulse to the 2708 PROGRAM input. While the data byte drives the 2708 data output lines and the PROGRAM PULSE is applied to the 2708, the pRDY line is held low forcing the CPU to wait until 192 usec has elapsed.

The PROGRAM ENABLE switches selectively enable programming by routing +12 volts to the $\overline{CS}$/WE input of a PROGRAM ENABLED socket when the switch is closed, or inhibit programming by applying +5 volts to the $\overline{CS}$/WE input of a PROGRAM DISABLED socket when the switch is open.

4.5 DMA CYCLES

The CPU acknowledges a DMA request by asserting the pHLDA line high. The system address, data out and control busses are then tri-stated allowing the DMA device to control these lines. The pHLDA signal to the BYTESAVER II is logically gated with switch settings DMA OVERRIDE ENABLE/DISABLE and DMA IN/OUT resulting in signal [IC1 pin 3] which ultimately either enables or disables the board thru node signal BOARD ENABLE. To enable the board, [IC1 pin 3] must be low. The table below shows the relationship among the DMA switches and signal [IC1 pin 3]. In the table, "Q" is output [IC26 pin 5] which is low when the board exists in an active memory bank (when the green LED is lit).

Table 3

DMA OVERRIDE	DMA IN/OUT	[IC1 PIN 3] (A LOW ENABLES THE BOARD)
DISABLED (OFF)	OUT (ON)	Q
DISABLED (OFF)	IN (OFF)	Q
ENABLED (ON)	OUT (ON)	(pHLDA) OR (Q)
ENABLED (ON)	IN (OFF)	(pHLDA) AND (Q)

From the table it is seen that when DMA OVERRIDE is disabled, the board must be placed in an active memory bank to be accessible, and the DMA IN/OUT switch setting is irrelevant. When DMA OVERRIDE is ENABLED, a DMA cycle will disable the board if DMA is OUT (since pHLDA is high); a DMA cycle will enable the board if DMA is IN regardless of the Q output state (since $\overline{\text{pHLDA}}$ is low). Thus, with DMA OVERRIDE enabled, a board with DMA OUT disappears during DMA transfers, and a board with DMA IN is available across memory bank boundries.

Section 5

ASSEMBLY INSTRUCTIONS

If you purchased a BYTESAVER II kit, you will find assembly to be straight-forward provided you follow the instructions below.

Before beginning assembly, verify you have all kit parts by referring to the Parts List. Please fill out and return the Missing Parts form to your authorized Cromemco dealer if any parts are damaged or missing.

5.1 ASSEMBLY STEPS

All parts are inserted from the component side of the board (with the white printed legend), and all soldering is done from the opposite side.

Be sure to use a high quality rosin core solder (DO NOT USE ACID CORE SOLDER), and a fine tipped low-wattage (25 W or less) soldering iron.

The printed legend on the component side of the board shows the exact location and orientation of each component (also see Figure 12). Carefully organize your work; check off each component after insertion and each assembly step when completed.

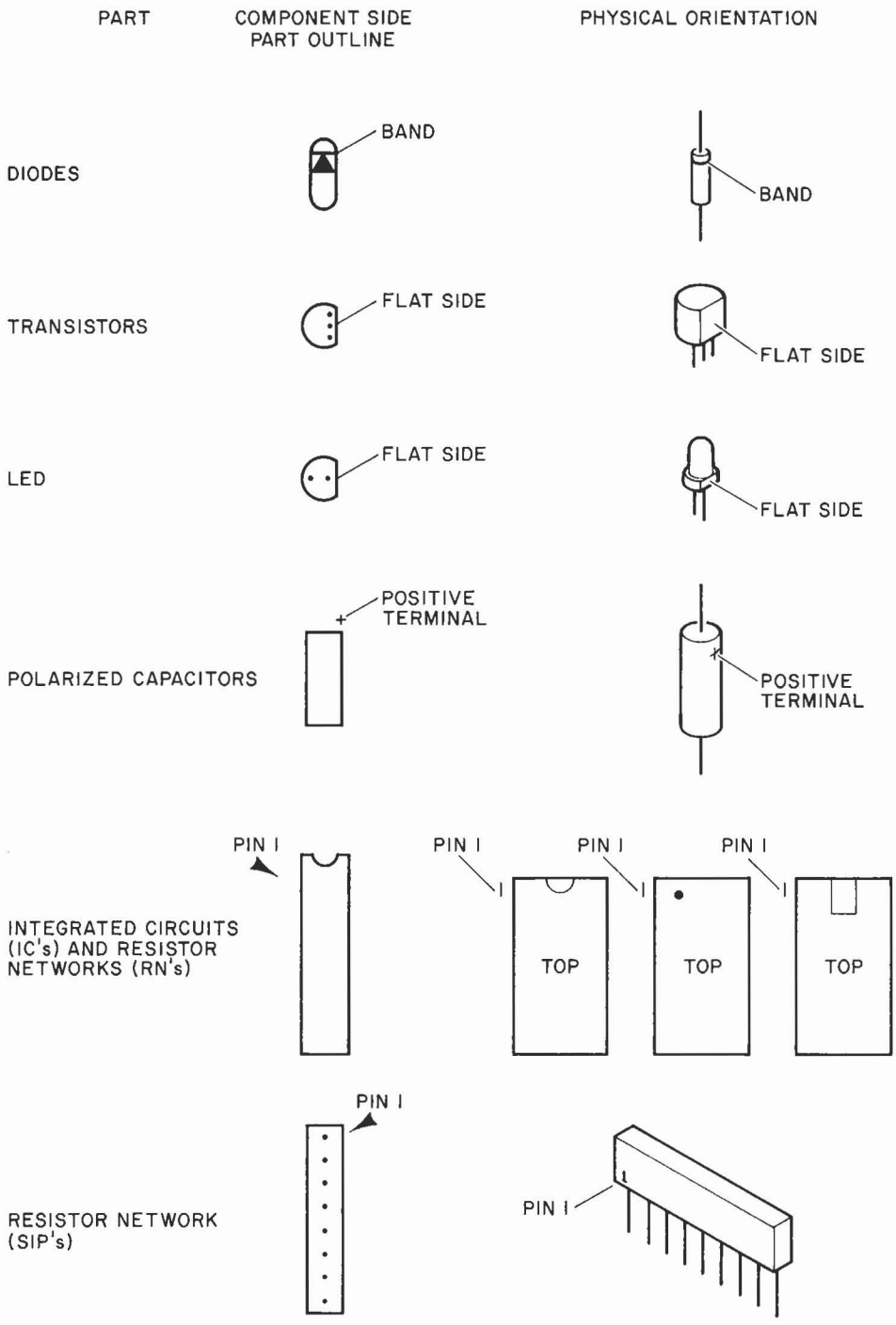


Figure 12: BYTESAVER II PART ORIENTATIONS

( ) Install transistors Q1 - Q21. Align transistor flat sides with outline drawings. Note that transistor types alternate between 2N3904 and 2N3906 up to Q17 and Q18, which are both 2N3904's.

( ) Install Zener diodes D19 (1N5254 3%) and D29 (1N5257). Align the bands on the diodes with the bands on the outline drawings. Install twenty-seven 1N4531 diodes D2 - D18, D20 - D28 and D30 in the same way.

( ) Solder in position all 1/4-watt resistors:

R1	180	BROWN-GREY-BROWN
R2-R3		NOT ASSIGNED
R4-R5	1K	BROWN-BLACK-RED
R6	100K	BROWN-BLACK-YELLOW
R7	1K	BROWN-BLACK-RED
R8	47	YELLOW-VIOLET-BLACK
R9	100	BROWN-BLACK-BROWN
R10	5.6K	GREEN-BLUE-RED
R11	10K	BROWN-BLACK-ORANGE
R12	5.6K	GREEN-BLUE-RED
R13-R14	1K	BROWN-BLACK-RED
R15		NOT ASSIGNED
R16-R17	150	BROWN-GREEN-BROWN
R18	1K	BROWN-BLACK-RED
R19-R22	150	BROWN-GREEN-BROWN

( ) Solder in position thirty-six IC sockets.

( ) Solder three SIP resistor networks RN2, RN5 and RN6 in place. The arrow tips printed on the circuit board point to SIP pin 1; align arrows with numerals "1" printed on SIP packages.

( ) Install seven polarized capacitors C1Ø - C11 and C23 - C27. WHEN INSTALLING THE 1Ø uF POLARIZED CAPACITORS MAKE CERTAIN THAT THE "+" END OF THE CAPACITOR IS ALIGNED WITH THE "+" PRINTED ON THE P.C. BOARD.

( ) Install the remaining forty-nine disc capacitors. The .Ø22 uF capacitors are labeled ".Ø22", and the smaller 22Ø pF capacitors are labeled "22Ø". Notice that C21 is a .Ø1 uF capacitor, not a .1 uF.

( ) Install transformer T1.

( ) Install light emitting diode D1. Align LED flat sides with outline drawings. Bend the LED leads at right angles so that the LED faces the top of the board when installed.

( ) Install three 8-pole DIP switches. The arrows on the switch packages indicating the ON position should point towards the top of the board.

( ) Install the SPDT toggle switch.

( ) Install IC16, the 7812 +12 volt regulator on the small heatsink in the lower left corner of the board. Secure with a steel screw and nut. Make sure the IC legs do <u>not</u> touch the metallic heat sink.

( ) Install IC2 and IC3 on the large heatsink in the upper right corner of the board. Position the mica insulating pad beneath IC2, the 79Ø5 -5 volt regulator; secure with a nylon screw inserted from the board solder side to a steel nut. Secure IC3, the 78Ø5 +5 volt regulator, with a steel screw and nut. Make sure the IC legs do not touch the metallic heat sink.

( ) Install all ICs and the three DIP Resistor Networks RN1, RN3 and RN4 in their correct sockets (see Important Note below). The arrow tips printed on the circuit board point to IC pin 1 (see Figure 12).

IMPORTANT NOTE

The most common assembly fault is bent under IC legs. To avoid this problem, first bend the IC legs to closely match the IC socket span. Then "rock" the IC into its socket with a gentle end-to-end pressure. Visually inspect the legs after insertion by looking beneath the device.

This completes the construction of the Cromemco BYTESAVER II board. Carefully inspect your work before proceeding. Take particular care to see that there are no inadvertent solder bridges between pads and/or adjacent foil

areas. It is a good practice to scrub the board solder side clean with a fluorocarbon solution to remove any fine metallic particles which may be imbedded in the rosin residue.

5.2 POWER LINE TESTING

Follow the next procedure to verify that no short circuits exist between the board power lines, or between the power lines and ground. If testing indicates a short circuit, the connection must be found and removed.

With the board disconnected from the S-1ØØ bus, connect an ohmmeter, on the R x 1 or lowest full-scale setting, across C25. The exact resistance reading is not important (it depends heavily on the ohmmeter design), but it should be several ohms or greater. If the reading indicates zero or a fraction of an ohm, a short exists between the +8 volt line and ground. Remove the short and verify by re-testing. Reverse the ohmmeter leads and again verify a non-zero ohm condition.

Test the +18 volt line as above by placing the ohmmeter leads across C26. Test the -18 volt line in the same way across C24.

Test the +5 volt line as above by placing the ohmmeter

leads across C11. Test the +12 volt line across C27. Test the -5 volt line across C1Ø. Test the +34.5 volt line across C23. In each case, observe a non-zero ohm condition.

Now, place the ohmmeter between the "+" end of polarized capacitor C11 and the "+" end of C27; repeat with C11 and C23; repeat with C27 and C23. Now place the ohmmeter leads between the "-" end of C1Ø and the "+" end of C11; then C23; then C27. Verify a non-zero ohm condition in each case.

Follow the next procedure to verify that proper power supply voltages are present when the BYTESAVER II is plugged into an S-1ØØ bus slot.

First, turn the system power OFF. Install the BYTESAVER II in an S-1ØØ slot which permits access to the component side of the board with a VOM. NEVER insert or remove the board or board parts with the system power ON.

Turn the system power ON. The BYTESAVER II switch settings are unimportant for this test. Carefully measure the voltage across C1Ø and verify 5.Ø volts with the same polarity as capacitor C1Ø. Carefully measure the voltage across C27 and verify 12.Ø volts with C27's polarity. Carefully measure the voltage across C1Ø and verify 12.Ø volts with the same polarity as C1Ø. Turn the PROGRAM POWER switch ON and carefully measure the voltage across C23.

Verify between 32.5 and 34.5 volts with C23's polarity.

This completes the preliminary testing of the BYTESAVER II board. If further testing indicates a board failure, the first corrective measure should be the removal of all board ICs and DIP resistor networks to check for bent under IC legs. If none are found, carefully re-insert the correctly oriented ICs in their proper sockets and refer to Section 4, or return the board to Cromemco for servicing (see WARRANTY at the end of this manual).

BYTESAVER II PARTS LIST

Integrated Circuits		Part No.
IC1	74LS00	010-0069
IC2	7905	012-0000
IC3	7805	012-0001
IC4	7406	010-0028
IC5	7406	010-0028
IC6	74LS02	010-0068
IC7	74LS05	010-0065
IC8	74LS05	010-0065
IC9	74LS33	010-0099
IC10	74367	010-0080
IC11	74LS05	010-0065
IC12	74LS05	010-0065
IC13	74LS00	010-0069
IC14	74LS04	010-0066
IC15	74LS74	010-0055
IC16	7812	012-0002
IC17	7406	010-0028
IC18	74LS02	010-0068
IC19	74LS42	010-0057
IC20	74367	010-0080
IC22	74LS136	010-0050
IC23	74367	010-0080
IC24	74367	010-0080
IC25	74LS33	010-0099
IC26	7474	010-0019
IC27	74393	010-0078
IC28	74LS42	010-0057

Resistor Networks		
RN1	4.7K, DIP	003-0017
RN2	1K, 10 PIN SIP	003-0011
RN3	18K, DIP	003-0019
RN4	18K, DIP	003-0019
RN5	1K, 8 PIN SIP	003-0007
RN6	1K, 8 PIN SIP	003-0007

IC Sockets	
8-SOCKETS, 24 PIN	017-0005
10-SOCKETS, 16 PIN	017-0002
18-SOCKETS, 14 PIN	017-0001

Capacitors		Part No.
C1-C9	.1 uF	004-0030
C10-C11	10uF @ 20V	004-0032
C12-C19	.05uF @25V	004-0027
C20	680 pF	004-0020
C21	.01 uF	004-0026
C22	.1 uF	004-0030
C23	10 uF @ 50V	004-0031
C24	6.8 uF @ 35V	004-0034
C25	10 uF @ 20V	004-0032
C26	6.8 uF @ 35V	004-0034
C27	10 uF @ 20V	004-0032
C28-C35	.022 uF	004-0023
C36-C38	.1 uF	004-0030
C39	220 pF	004-0013
C40	.1 uF	004-0030
C41	220 pF	004-0013
C42	.1 uF	004-0030
C43-C45	220 pF	004-0013
C46	.1 uF	004-0030
C47	220 pF	004-0013
C48-C49	.1 uF	004-0030
C50	220 pF	004-0013
C51-C52	.1 uF	004-0030
C53	220 pF	004-0013
C54-C55	.1 uF	004-0030
C56	220 pF	004-0013

Diodes		
D1	LED TIL-211	008-0020
D2-D18	1N4531	008-0002
D19	1N5254 3%	008-0004
D20-D28	1N4531	008-0002
D29	1N5257	008-0003
D30	1N4531	008-0002

BYTESAVER II PARTS LIST

Resistors		Part No.
R1	180	001-0009
R2-R3	NOT	ASSIGNED
R4-R5	1K	001-0018
R6	100K	001-0039
R7	1K	001-0018
R8	47	001-0003
R9	100	001-0007
R10	5.6K	001-0026
R11	10K	001-0030
R12	5.6K	001-0026
R13	1K	001-0018
R14	1K	001-0018
R15	NOT	ASSIGNED
R16-R17	150	001-0008
R18	1K	001-0018
R19-R22	150	001-0008

Capacitors		Part No.
Q1	2N3904	009-0001
Q2	2N3906	009-0002
Q3	2N3904	009-0001
Q4	2N3906	009-0002
Q5	2N3904	009-0001
Q6	2N3906	009-0002
Q7	2N3904	009-0001
Q8	2N3906	009-0002
Q9	2N3904	009-0001
Q10	2N3906	009-0002
Q11	2N3904	009-0001
Q12	2N3906	009-0002
Q13	2N3904	009-0001
Q14	2N3906	009-0002
Q15	2N3904	009-0001
Q16	2N3906	009-0002
Q17	2N3904	009-0001
Q18	2N3904	009-0001
Q19	2N3906	009-0002
Q20	2N3904	009-0001
Q21	MPS-6560	009-0021

Miscellaneous	
3 DIP SWITCHES, 8 POLE	013-0002
1 TOGGLE SWITCH	013-0000
1 LARGE HEAT SINK	021-0017
1 SMALL HEAT SINK	021-0016
1 XT8K XFMR.	014-0001
4 SCREWS, 6-32 STEEL	015-0008
1 SCREW, 6-32, NYLON	015-0002
5 HEX NUTS, 6-32	015-0013
1 INSULATING PAD	999-0000
1 PC BOARD	020-0003

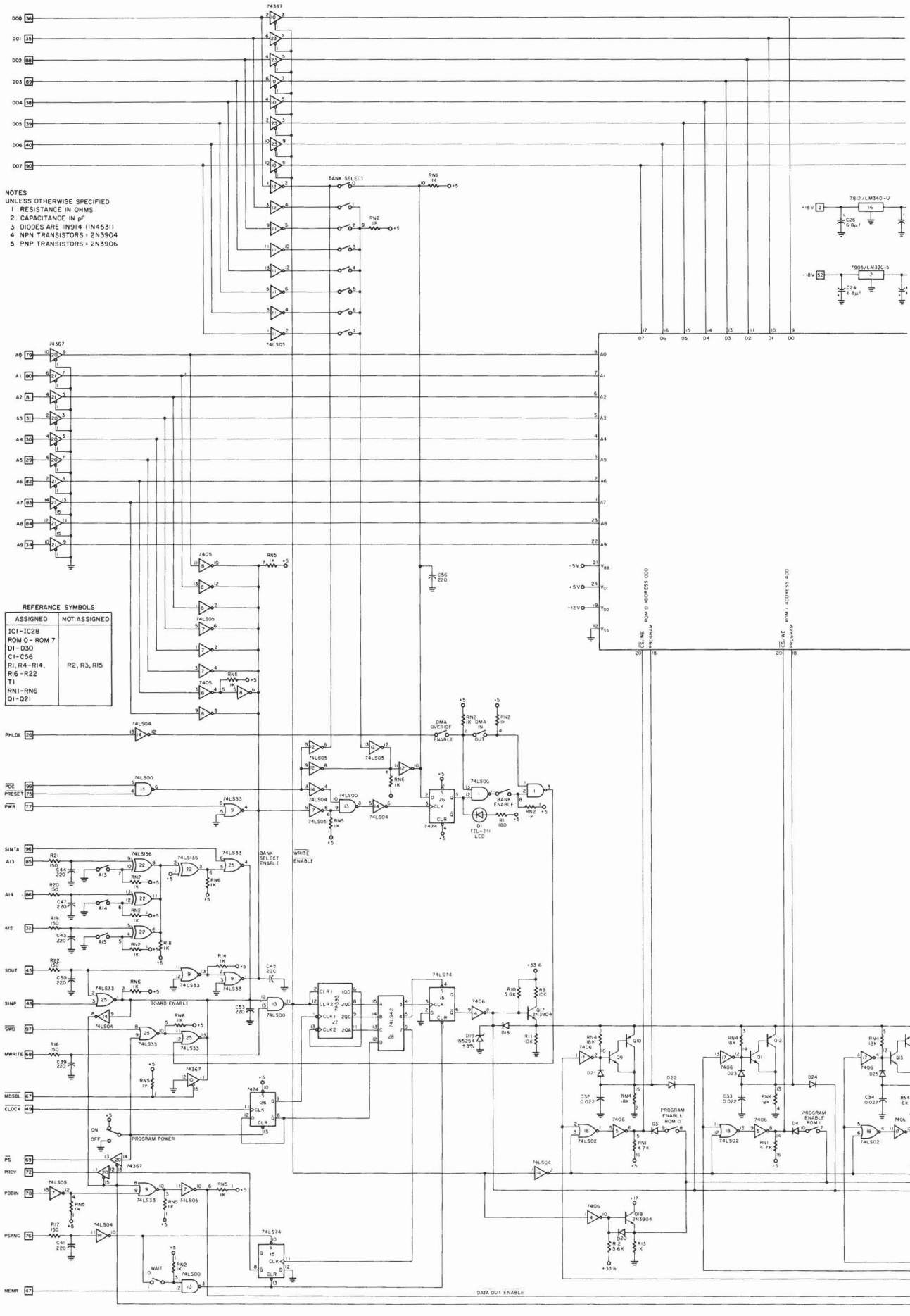
Documentation	
BYTESAVER II INSTRUCTION MANUAL	023-0001

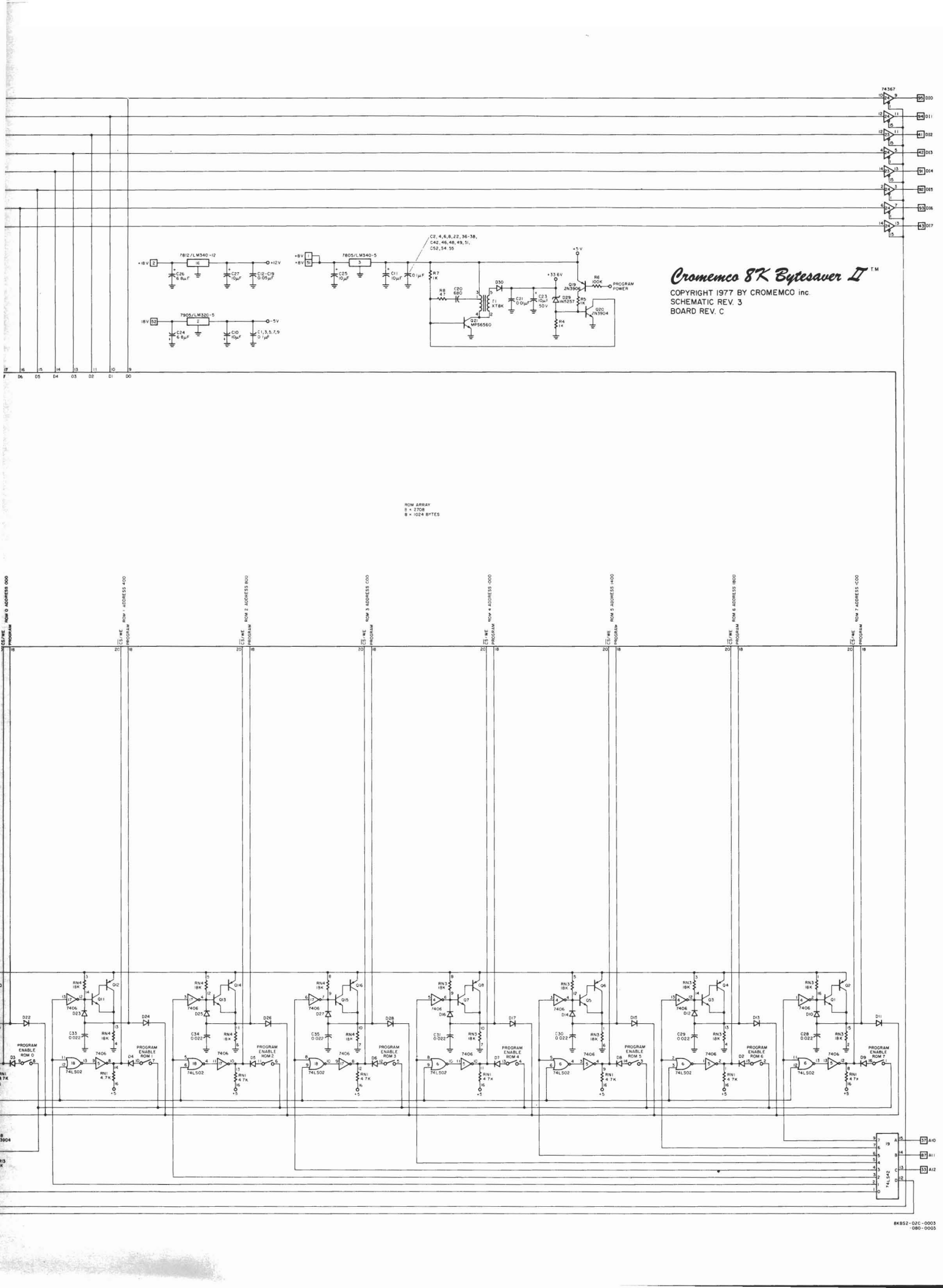
WARRANTY

Your factory built BYTESAVER II is warranted against defects in materials and workmanship for a period of 90 days from the date of delivery. We will repair or replace products that prove to be defective during the warranty period provided they are returned to Cromemco. No other warranty is expressed or implied. We are not liable for consequential damages.

Should your factory built BYTESAVER II fail after the warranty period, it will be repaired for a fixed fee, provided it is returned to Cromemco. We reserve the right to refuse to repair any product which has, in our opinion, been subjected to abnormal electrical or mechanical abuse. The service fee is currently $70.00, and is subject to change without notice.

Your assembled BYTESAVER II kit will be repaired for a fixed fee, provided it is returned to Cromemco. We reserve the right to refuse repair of any kit which has not, in our opinion, been assembled in a workmanlike manner, or has been subjected to abnormal electrical or mechanical abuse. Payment of the service fee must accompany the returned merchandise. The service fee for kit repair is currently $70.00, and is subject to change without notice.


NOTES
UNLESS OTHERWISE SPECIFIED
1. RESISTANCE IN OHMS
2. CAPACITANCE IN pF
3. DIODES ARE 1N914 (1N4531)
4. NPN TRANSISTORS = 2N3904
5. PNP TRANSISTORS = 2N3906
REFERANCE SYMBOLS
ASSIGNED
NOT ASSIGNED
IC1-IC28
ROM 0 - ROM 7
D1-D30
C1-C56
R1, R4-R14, R16-R22
T1
RN1-RN6
Q1-Q21
R2, R3, R15
BANK SELECT
PROGRAM POWER
BOARD ENABLE
BANK SELECT ENABLE
WRITE ENABLE
DATA OUT ENABLE
PROGRAM ENABLE ROM 0
PROGRAM ENABLE ROM 1
ROM 0 ADDRESS 000
ROM 1 ADDRESS 400
DMA OVERIDE ENABLE
BANK ENABLE
WAIT
ON
OFF
7812/LM340-12
7905/LM320L-5
74367
74LS05
74LS04
74LS00
74LS33
74LS136
74LS74
74LS42
74LS93
74LS02
7405
7406



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